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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,035	04/20/2007	Tadahiro Ohmi	5016-0103PUS1	5997
2292	7590	03/12/2010	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				CALEY, MICHAEL H
ART UNIT		PAPER NUMBER		
		2871		
NOTIFICATION DATE			DELIVERY MODE	
03/12/2010			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/581,035	OHMI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	MICHAEL H. CALEY	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 18 December 2009.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.  
 4a) Of the above claim(s) 12-22 and 26-31 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-11 and 23-25 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 30 May 2006 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)               |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application     |
| Paper No(s)/Mail Date <u>5/30/06; 6/15/07</u> .  | 6) <input checked="" type="checkbox"/> Other: <u>WO 03/03454 A1</u> . |

## **DETAILED ACTION**

### ***Election/Restrictions***

Claims 12-22 and 26-31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/18/09.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1-5, 8-10, 23, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Furusawa (U.S. Patent Application Publication No. 2004/0005739).**

Regarding claims 1 and 23, Furusawa discloses an active matrix display device having a plurality of thin film transistors (Figures 1-2; Paragraphs [0054]-[0055]) disposed in a matrix on an insulating substrate (Figure 3 element 10) and wiring (e.g. Figures 1-3 element 26) connected to these thin film transistors;

wherein said active matrix display device comprises a flattening layer (20) surrounding said wiring, and

a surface of said wiring and a surface of said flattening layer form substantially the same plane (Figures 3, 8 elements 20, 26; Paragraph [0095]).

Regarding claims 2 and 24, Furusawa discloses said wiring as including gate wiring (12, 13), source wiring (26), and drain wiring (28 or 24),

said gate wiring constituting scanning lines (12) connected to gate electrodes of said thin film transistors,

said source wiring and drain wiring being respectively connected to source electrodes and drain electrodes (22) of said thin film transistors,

one of said source wiring and said drain wiring constituting signal lines (26) adapted to supply signals to said thin film transistors while the other (28) is connected to pixel electrodes (24),

and wherein said flattening layer (20) surrounds said source electrodes, said drain electrodes, and said source wiring, and said drain wiring (Figure 3),

surfaces of said source electrodes (22), said drain electrodes (22), said source wiring (26), and said drain wiring (28), and the surface of said flattening layer forming substantially the same plane (Figure 3).

Regarding claims 3 and 4, Furusawa discloses the flattening layer as formed of a photosensitive resin composition (Paragraphs [0082], [0083]).

Regarding claim 5, Furusawa discloses the flattening layer as comprising an inorganic substance (e.g. metal oxide, Paragraph [0082]).

Regarding claims 8 and 9, Furusawa discloses the insulating substrate as formed of a transparent material (Paragraph [0054]) and having a surface covered with an insulator (e.g. element 16, Paragraph [0075]).

Regarding claim 10, Furusawa discloses the display device as a liquid crystal display device (Paragraph [0002]).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa in view of Miyaki et al. (WO 03/033454 A1 "Miyaki").**

U.S. Patent No. 6,846,890 is used as an English language equivalent of the Miyaki publication.

Regarding claim 6, Furusawa discloses the resin as having a radiation sensitive component (Paragraphs [0082], [0083]), but fails to disclose the particular resin composition. Miyaki, however, teaches an alkali-soluble alicyclic olefin resin insulator composition (Column 1 lines 37-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the flattening layer from the proposed resin composition. One would have been motivated to form the flattening layer from the resin composition to benefit from its known advantages for display use, such as high transparency and a high level of electrical insulation, etc. (Miyaki: Column 1 lines 73-55).

**Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa in view of Ishihara et al. (U.S. Patent Application Publication No. 2002/0012080 "Ishihara").**

Furusawa discloses the source wiring and the drain wiring as each containing an organic substance (Paragraphs [0095], [0096]), but fails to disclose the source electrodes and drain electrodes as containing an organic substance. Ishihara, however, teaches replacing amorphous silicon source and drain electrodes with an organic semiconductor film (Paragraphs [0003] and [0036]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the source and drain electrodes to contain an organic substance. One would have been motivated to form the source and drain electrodes with an organic substance to reduce the TFT panel production cost according to conventional means (Ishihara: Paragraph [0003]).

**Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa in view of Tanaka et al. (U.S. Patent No. 6,933,180 "Tanaka").**

Furusawa fails to disclose the display device as an organic EL display device. Tanaka, however, teaches TFT array substrates as interchangeably implemented as for an organic EL display or a liquid crystal display (abstract; Column 1 lines 7-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the TFT array substrate as an organic EL display. One would have been motivated to form the display as an organic EL display to benefit from known advantages such as the lack of need for a separate light source that is necessary in liquid crystal displays.

**Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furusawa in view of Chino (U.S. Patent Application Publication No. 2004/0027056).**

Furusawa discloses an insulation film (16) provided to surround the gate electrodes and gate wiring, but fails to disclose the gate electrodes, gate wiring, and insulation film as forming substantially the same flat surface, and a gate insulation film as formed on the flat surface. Chino, however, teaches such a gate electrode and wiring (Figures 1 and 2 element 35), insulation film (55), and gate insulation film (9) layered structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an insulation film to surround and form a flat surface with the gate electrodes and wiring and to form a gate insulating film over the flat surface. One would have been motivated to form the gate wiring and insulating films as proposed to improve insulation between the gate electrode and source/drain electrodes (Chino: Paragraphs [0013], [0027]).

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 6:00 a.m - 2:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871